Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application, where added material is shown in underlined type, deleted material is shown in ~~strikeout type~~:

Listing of Claims:

1. (Currently amended) A device for data stream analyzing, comprising a processor means, ~~and~~ a program memory, and a multiplexable data stream delayline for receiving a data stream; said device for enabling parsing of ~~making it possible to parse a~~ said data stream in a way that is controlled by an interchangeable program.

2. (Currently amended) A device according to claim 1, further comprising a ~~multiplexable data stream delayline for receiving said data stream, and~~ multiplexing means for connecting different parts of ~~the~~ said data stream to said processor means.

3. (Currently amended) A device according to claim 2, wherein the multiplexing means includes a multiplexing control means for automatically keeping track of where specific data is located in the delayline~~,~~ and for enabling at least one program to start executing once the data is received in the delayline ~~making it possible to write programs for controlling the device that can start executing at any time after the data have arrived to the device, and without the need for starting execution at a specific time relative to when the data stream was entering the device~~.

4. (Previously presented) A device according to claim 2, wherein said delayline comprises a 23 shift deep, 1 byte wide shift register.

5. (Currently amended) A device according to claim 3, wherein the multiplexing control means automatically keeps track of where specific data is located in the delayline by the use of a first and second position register that change in a predetermined way ~~according to certain rules~~ when a packet is forwarded in the delayline.

6. (Currently amended) A device according to claim 5, wherein values of the position registers are changed in the following ~~way;~~ way: when a packet arrives, the first register starts to increment for every byte; when the packet has come to its end where the packets DV (data valid) signal becomes false again, the first register stops counting and the second register starts to increment.

7. (Currently amended) A device ~~according to claim 5~~ for data stream analyzing, comprising a processor means, a program memory, and a multiplexable data stream delayline for receiving a data stream, said device for enabling parsing of said data stream in a way that is controlled by an interchangeable program; further comprising a multiplexing means for connecting different parts of said data stream to said processor means; wherein the multiplexing means includes a multiplexing control means for automatically keeping track of where specific data is located in the delayline and for enabling at least one program to start executing once the data is received in the delayline; wherein the multiplexing control means automatically keeps track of where specific data is located in the delayline by the use of a first and second position register that change in a predetermined way when a packet is forwarded in the delayline; and wherein said device ~~which~~ automatically keeps track of where specific data is located in the delayline, by the use of said dedicated position registers together with the use of a formula

$$P = tagfield + lastfield - wanted\_tag$$

and "P" is the position of a wanted byte in the delayline; "tagfield" is the value of the first register; "lastfield" is the value of the second register and "wanted_tag" is the position of the wanted byte relative to the beginning of the packet.

8. (Currently amended) A device according to claim 1, further comprising a plurality of registers for performing operations ~~making logical and/or arithmetic operations~~ on data-stream data, before an actual comparison of the data with other data is executed.

9. (Previously presented) A device according to claim 1, further comprising a stack memory means which enables the writing of one or more programs with subroutines for reducing the need for large program memories.

10. (Currently amended) A device according to claim 1, further comprising a base address register for the processor means for enabling code to be reused ~~to make it possible to reuse code~~ to recognize a given pattern even if ~~it~~ the given pattern starts at different positions in the data stream.

11. (Previously presented) A device according to claim 1, wherein the program memory is of double ported type.